FIG. **2** illustrates a circuit layout of a monolithic PIC according to one embodiment of the present invention. The PIC of FIG. **2** is fabricated on a semiconductor die **20** and includes a first output HVFET **23** having a set of relatively short interdigitated source/drain segments, and a second output HVFET **24** having a set of relatively long interdigitated source/drain segments. The segments of HVFETs **23** & **24** are placed on die **20** in a manner that optimizes the layout of control circuit **21**. The arrangement of HVFETs **23** & **24** also improves the layout of the complete PIC such that die **20** has a lower aspect ratio as compared to prior art devices, even for implementations with low current handling capability.

As can be seen, output HVFET **23**, with the short segments, is located on die **20** adjacent the short, lateral side of control circuit **21**. Control circuit **21** and HVFET **23** both have substantially the same width (W_1). In this embodiment, HVFET **23** has a length (L_1) that is less than the length (L_2) of control circuit **11**. The total length (L) of semiconductor die **20** is approximately equal to the sum of the lengths of HVFET **23** and control circuit **21** ($L \simeq L_1+L_2$).

In the embodiment of FIG. **2**, output HVFET **24** is shown located on die **20** adjacent the long, bottom side of control circuit **21**, and also extending beneath the length of HVFET **23**. The length of the segments of output HVFET **24** is substantially equal to the length (L_2) of control circuit **21** plus the length (L_1) of the segments of output HVFET **23**. In other words, the short HVFET segments are placed alongside the short side of control circuit **11** such that the combined control circuit and short HVFET segment length is substantially the same as the length of the long HVFET segments of transistor **24**.

The total width (W) of semiconductor die **20** is approximately equal to the sum of the widths of control circuit **21** and HVFET **24** ($W \simeq W_1+W_2$). To manufacture a PIC device with increased current handling capability, more long segments are added in parallel to HVFET **24**, which has the effect of increasing the W_2 dimension and lowering the aspect ratio of semiconductor die **20**.

Practitioners in the integrated circuit and semiconductor fabrication arts will appreciate that the embodiment shown in FIG. **2** permits control circuit **21** to have a layout with a smaller aspect ratio than prior art designs. In the implementation shown in FIG. **2**, the length (L_2) of control circuit **21** is about three times its width (W_1). Furthermore, the novel use and placement of multiple HVFETs having different segment lengths results in an aspect ratio closer to 1.0 for the complete PIC. This means that a family of PIC devices, each with different current handling capability, may be manufactured on a semiconductor die **20**, each having an aspect ratio closer to 1.0. For the embodiment shown in FIG. **2**, the aspect ratio of die **20** is about 1.6.

With continuing reference to FIG. **2**, a PIC device having a relatively small current handling capability may be realized by connecting control circuit **21** to HVFET **23**, but not to HVFET **24**. A PIC device having increased current handling capability may be implemented by connecting control circuit **21** to both HVFET **23** and HVFET **24**, or just to HVFET **24** and not HVFET **23**. PIC devices that provide even larger current handing capability may be realized by increasing the number of long segment of HVFET **24** during the layout and manufacturing of semiconductor die **20**. In each case, the dimensions of control circuit **21** remain the same. In accordance with the present invention, a complete family of PIC devices having a wide range of current handling capabilities may be implemented on a semiconductor die having an aspect ratio within a range of 0.5 to 2.0.

It should be understood that even though the embodiment of FIG. **2** illustrates two HVFETs with different length segments, there is no restriction on the number of HVFETs that may be included on die **20**. That is, more than two HVFETs having different length segments may be included on die **20**.

For example, a PIC with four output HVFETs may be implemented in which two additional HVFETs are located side-by-side on die **20** above or below HVFET **24**. The two additional output HVFETs may have a combined segment length that is approximately equal to the sum of the lengths of HVFET **23** and control circuit **21** ($L \simeq L_1+L_2$). In such as case, the segment lengths of the two additional HVFETS may have an intermediate length that is longer than that of the short segments of HVFET **23**, yet shorter than the length of the long segments of HVFET **24**. These additional HVFETs with intermediate length segments may be selectively coupled to control circuit **21** to implement a PIC device providing an intermediate range of output current capacity.

FIG. **3** is a circuit schematic diagram that corresponds to the monolithic power integrated circuit shown in FIG. **2**. As explained previously, control circuit **21** may be selectively coupled to output HVFET **23** or to output HVFET **24**, or to both HVFETs **23** & **24**. This latter case is depicted by the dashed line showing a common connection to each of the three terminals (i.e., source, drain, and gate) of the respective HVFETs. Alternatively, the HVFETs may have only one or two terminals coupled together (i.e., only the source terminals).

Persons of ordinary skill in the integrated circuit and semiconductor arts will appreciate that selective coupling between control circuit **21** and one or both of the output HVFETs **23** & **24** may be achieved utilizing a variety of conventional techniques and circuits. For example, an optional metal connection may be implemented during the layout and fabrication of the PIC. Alternatively, an ordinary on-chip switching circuit may be utilized for selectively coupling one or more of the output HVFETs to control circuit **21**. This switching circuit may be incorporated into the layout of control circuit **21** and may comprise one or more transistor switching devices (e.g., transmission gates).

Although the present invention has been described in conjunction with specific embodiments, those of ordinary skill in the arts will appreciate that numerous modifications and alterations are well within the scope of the present invention. Accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense.

I claim:

1. A method of manufacturing a monolithic power integrated circuit (PIC) on a semiconductor die, the method comprising:

locating a control circuit in a first area of the semiconductor die, the control circuit having a length that extends along a first side and a width that extends along a second side;

locating a first output high voltage field-effect transistors (HVFET) adjacent the second side of the control circuit, the first output HVFET having a width substantially equal to the width of the control circuit;

locating a second output HVFET adjacent the first side of the control circuit, the second output HVFET having a length substantially equal to the length of the control circuit plus a length of the first output HVFET; and

coupling the control circuit to at least one of the first or second output HVFETs.